REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-22, 24-25, 27, 56-64, 66-76, and 79-83 are pending in the application. The Examiner additionally stated that claims 1-22, 24-25, 27, 56-64, 66-76, and 79-83 are rejected. By this communication, claims 1 and 5t6 are amended. Hence, claims 1-22, 24-25, 27, 56-64, 66-76, and 79-83 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1-6, 11-12, 24-25, 27, 56-60, 66, and 79-83 under 35 U.S.C. 103(a) as being unpatentable over Kessler et al., U.S. Patent 6,789,147 (hereinafter, Kessler) in view of Bakhle et al., U.S. Patent 6,021,201 (hereinafter, Bakhle), in view of Best, U.S. Patent 4,278,837, (hereinafter, Best). Applicant respectfully traverses the Examiner's rejections.

Claim 1 recites:

1. A microprocessor apparatus, for performing a cryptographic operation, the apparatus comprising:

an x86-compatible microprocessor, comprising:

fetch logic, configured to fetch an application program from memory for execution by said x86-compatible microprocessor, said application program comprising:

an atomic instruction, configured to direct said x86-compatible microprocessor to perform the cryptographic operation, wherein said atomic instruction comprises:

an opcode field, configured to prescribe that said x86-compatible microprocessor accomplish the cryptographic operation as further specified within a control word stored in said memory; and

a repeat prefix field, coupled to said opcode field, configured to indicate that the cryptographic operation prescribed by the atomic instruction is to be accomplished on a plurality of blocks of input data;

a cryptography unit, configured to execute a plurality of cryptographic rounds on each of a plurality of input text blocks to generate a corresponding each of a plurality of output text blocks, wherein said plurality of cryptographic rounds are prescribed by said control word; and

an x86 integer unit, an x86 floating point unit, an x86 MMX unit, and an x86 SSE unit, wherein said cryptography unit operates in parallel with said x86 integer unit, said x86 floating point unit, said x86 MMX unit, and said x86 SSE unit, to accomplish the cryptographic operation.

Nowhere does the cited art disclose **an x86 integer unit, an x86 floating point unit, an x86 MMX unit, and an x86 SSE unit, wherein said cryptography unit operates in parallel with said x86 integer unit, said x86 floating point unit, said x86 MMX unit, and said x86 SSE unit, to accomplish the cryptographic operation**, as is recited in claim 1. Clearly, the cited art fails to disclose a x86-compatible microprocessor comprising the noted elements. Kessler utterly fails to teach any form of microprocessor whatsoever. Bakhle fails to teach any form of an x86-compatible microprocessor as is

recited according to the above limitation. The microprocessor of Best (Fig. 17, 100) is void of any of the recited elements as well. *None* of the references teach or suggest an x86 integer unit, x86 floating point unit, x86 MMX unit, or x86 SSE unit. Consequently, it is inconceivable that they would suggest "wherein said cryptography unit operates in parallel with said x86 integer unit, said x86 floating point unit, said x86 MMX unit, and said x86 SSE unit, to accomplish the cryptographic operation."

Applicant has amended the independent claims to recite additional elements that distinguish the x86-compatible microprocessor according to the present invention from that which the Examiner has asserted is inferred by the Best reference. Best could not have contemplated a superscalar architecture as is recited in the independent claims by virtue of the noted elements operating in parallel, for such an architecture did not exist at the time of invention. This fact is corroborated by the Examiner's own submission of the Wikipedia reference entered on 06/04/2008 (page 4, paragraphs 3 and 4).

In traversal of the Examiner's statement that the "indivisible microprocessor that behaves in exactly the same manner as the 'microprocessor' of the instant application," Applicant submits that this is not what Best discloses. Rather, Best discloses that "hybrid device 104 in FIG. 17 *may* perform as a whole like a conventional microprocessor *except* for the fact that the program it executes, which is stored in RAM 12, is in cipher." (col. 19, lines 31-34). The Examiner's assertion is not equivalent to that which is taught by Best. The microprocessor of Best existed nearly 20 years before superscalar architectures, in fact, years before floating point coprocessors were incorporated into the x86-architecture, one skilled in the art would be compelled to acknowledge that Best's microprocessor *may* perform as a whole like a conventional microprocessor of that time period—prior to parallel operation of individual execution units, as is argued above. It is not reasonable to argue that the reference would suggest limitations as architecturally significant as superscalar technology.

Applicant furthermore notes in response to Examiner's arguments that any combination of any type of cryptographic coprocessor with any conventional microprocessor would still yield a mere hybrid circuit that deciphers and application program for execution by

the conventional microprocessor, which does not meet the limitation that "wherein said cryptography unit operates in parallel with said x86 integer unit, said x86 floating point unit, said x86 MMX unit, and said x86 SSE unit, to accomplish the cryptographic operation."

In traversal of the Examiner's Official Notice, Applicant submits that it is a well known fact that the x87 math coprocessor was not incorporated into the same unit as the processing unit until production of the 80486 in 1989, a full ten years after the filing date of the Best reference. Thus, there is no prior art teaching where any form of coprocessor had been integrated into an x86-compatible microprocessor. What Best suggests is hybridization of two separate chips. Even in the broadest interpretation of Best's teaching, the result would yield nothing more than a hybridization of a non-superscalar x86-compatible processor (lacking all of the elements recited in claim 1) with whatever "coprocessor" is chosen.

Accordingly, since Applicant has shown that the cited art utterly fails to disclose the elements noted above, it is submitted that the rejection of claim 1 is overcome. Consequently, for at least the reasons argued above, Applicant respectfully asserts that claim 1 is both novel and nonobvious, and it is respectfully requested that the rejection be withdrawn.

Claim 56 recites substantially the same elements and limitations as are argued above as being allowable over the prior art of record, and consequently Applicant respectfully asserts that claim 56 is both novel and nonobvious as well, and it is thus requested that the rejection of this claim be withdrawn. Traversal of the Official Notice taken is made as well and reference is made to the arguments in traversal of the same subject matter with reference to claim 1.

With respect to claims 2-6, 11-12, 24-25, 27, 56-60, 66, and 79-83, these claims depend from claims 1 and 56 as appropriate, and add further limitations that are neither anticipated nor made obvious by the cited references. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 2-6, 11-12, 24-25, 27, 56-60, 66, and 79-83.

The Examiner rejected claims 7-10 and 61-64 under 35 U.S.C. 103(a) as being unpatentable over Kessler in view of Bakhle in view of Best, as noted above, and further in view of "Applied Cryptography, 2nd Edition."

Applicant respectfully traverses the Examiner's rejections and notes that claims 7-10 and 61-64, depend from claims 1 and 56, respectively, and add further limitations over that subject matter which is argued above as being allowable over the prior art of record. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 7-10 and 61-64.

The Examiner additionally rejected claims 13-22 and 67-76 under 35 U.S.C. 103(a) as being unpatentable over Kessler in view of Bakhle in view of Best, and further in view of Johns-Vano et al. (U.S. Patent 6,026,490). Applicant respectfully traverses and notes that claims 13-22 and 67-76 depend from claims 1 and 56, respectively, and add further limitations over that subject matter which is argued above as being allowable over the prior art of record. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 13-22 and 67-76.

CONCLUSIONS

Applicant believes this to be a complete response to all of the issues raised in the instant office action and further submits, in view of the amendments and arguments advanced above, that claims 1-22, 24-25, 27, 56-64, 66-76, and 79-83 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant also notes that any amendments made by way of this response, and the observations contained herein, are made solely for the purpose of expediting the patent application process in a manner consistent with the PTO's Patent business Goals (PBG), 65 Fed. Reg. 54603 (September 8, 2000), and are furthermore made without prejudice to Applicant under this or any other jurisdictions. It is moreover asserted that insofar as any subject matter might otherwise be regarded as having been abandoned or effectively disclaimed by virtue of amendments made herein and/or incorporated in attachments submitted with this response, Applicants wishes to reserve the right and hereby provides notice of intent to restore such subject matter and/or file a continuation application in respect thereof.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,
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